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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DANG, KHANH	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 07/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/966,095	BALAY ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-8,10-12,14-17,19-21 and 23-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-8,10-12,14-17,19-21 and 23-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Background

The examiner's answer dated 3/2/2006 contains a new ground of rejection. As set forth in the examiner's answer, appellant must within TWO MONTHS from the date of this answer exercise one of the following two options to avoid *sua sponte* **dismissal of the appeal** as to the claims subject to the new ground of rejection:

(1) **Reopen prosecution.** Request that prosecution be reopened before the primary examiner by filing a reply under 37 CFR 1.111 with or without amendment, affidavit or other evidence. Any amendment, affidavit or other evidence must be relevant to the new grounds of rejection. A request that complies with 37 CFR 41.39(b)(1) will be entered and considered. Any request that prosecution be reopened will be treated as a request to withdraw the appeal.

(2) **Maintain appeal.** Request that the appeal be maintained by filing a reply brief as set forth in 37 CFR 41.41. Such a reply brief must address each new ground of rejection as set forth in 37 CFR 41.37(c)(1)(vii) and should be in compliance with the other requirements of 37 CFR 41.37(c). If a reply brief filed pursuant to 37 CFR 41.39(b)(2) is accompanied by any amendment, affidavit or other evidence, it shall be treated as a request that prosecution be reopened before the primary examiner under 37 CFR 41.39(b)(1).

In a communication filed 5/1/2006, appellant requested that prosecution be reopened before this primary examiner without any amendment.

The examiner maintains the rejections set forth in the Final Rejection and Examiner' Answer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 6- 8, 10-12, 15-17, 19-21, 24- 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tal in view of Lucent Technologies.

With regard to claim 1, Tal discloses a system for interconnectlng two or more computer bus architectures (the compact PCI (Peripheral Component Interconnect) shown generally at Fig. 8, for example), comprising: a first bus segment (PCI bus segment 802, column 6, lines 43-64, for example) to transmit data information, a first half bridge circuit (the PCI serializer on system card 810 in segment 802, Fig. 8, and shown in details as PCI serilalizer 700 on segment 802, Fig. 7, column 6, lines 28-38; note that the extra serializer in card 806 on PCI bus segment 802, showed in Fig. 8, are

only for redundancy; note also that the circuit 700, Fig. 7, corresponds to the half bridge disclosed by the Applicant in the originally filed specification, page 1, lines 12-17; page 6, lines 20-26, page 7, line 1 to page 9, line 4; and particularly Fig. 2.) connected to said first bus segment (PCI bus segment 802, column 6, lines 43-64, for example), said first half bridge circuit (PCI serializer 700, shown at Fig. 7, on segment 802 side, Fig. 8) comprising a first DMA circuit (704, Fig. 7, column 6, lines 28-28); a second bus segment (PCI bus segment 804, column 6, lines 43-64, for example) to transmit data information; a second half bridge circuit (the PCI serializer on card 812 in segment 804, Fig. 8, and shown in details as PCI serilalizer 700 on segment 804, Fig. 7, column 6, lines 28-38; note that the extra serializer in card 808 on PCI bus segment 804, showed in Fig. 8, are only for redundancy) connected to said first half bridge circuit (700, shown at Fig. 7, on segment 802 side), said second half bridge circuit (700, shown at Fig. 7, on segment 804 side) comprising a second DMA circuit (704, Fig. 7) and transferring data information between said first bus segment (segment 802, column 6, lines 43-64, for example), and said second bus segment (segment 804, column 6, lines 43-64, for example). Tal further discloses that the serial channel (having a plurality of data paths connecting the first half bridge to the second half bridge) is built out of 4 full duplex pairs, each providing 622 mbps of bandwidth. See column 6, lines 18-27. As disclosed by the Applicants in the originally filed specification, page 6, lines 5-8, and lines 20-26, "the first half bridge circuit 4 is connected with the second half bridge circuit 6 by four full duplex high speed serial data lines 5 each having a bandwidth of 622 Mb/s" (emphasis added).

However, Tal does not disclose that the serial channel comprising 4 full duplex pair can be "scalable" depending on a bandwidth needed for a particular application. To define the term "scalable", Applicants cited page 10, lines 6-10 of originally filed specification, which states that "[a]lthough the present invention is described with reference to embodiments teaching four high speed serial data lines running between two half bridge circuits, the principles of the present invention are equally applicable to the addition or subtraction of high speed serial data lines depending upon the bandwidth needed between two half bridge circuits." See Appeal Brief, Summary of the Invention, last three lines.

Lucent Technologies discloses the use of the ORT4622 half bridge (page 1, 4th paragraph) including field programmable gate arrays (FPGAs), see page 1, 1st paragraph, and containing "a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used), see page1, 4th paragraph, for providing design flexibility, functionality, and performance. See page 1, 1st and 5th paragraphs. The ORT4622 half bridge is clearly "scalable" depending on the bandwidth needed. The fact that the ORT4622 half bridge contains "a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used)" (emphasis added) clearly indicates that less than 4 channels can be used when less bandwidth is needed. As a matter of fact, the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ. Applicants clearly disclose that "[t]he first and second half bridge circuits, 4 and 6, would consist of an ORT4622 Lucent FPSC (Field Programmable System Chip) which implements a 2.5 Gb/s physical (LVDS Serial I/Os with clock recovery) and transport

layers together with a PCI controller. Although the ORT4622 is shown, any number of components supporting high speed data transfer between bus segments could be used to implement the invention." See Figs 1 and 2, and Applicants' originally filed specification, page 6, lines 20-26. Since the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ, it is clear that the serial data paths provided by the two ORT4622 half bridges are "scalable" depending on a bandwidth needed.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the ORT4622 half bridge, as taught by Lucent Technologies, to replace the half bridge 700 (Figs. 7 and 8) on each side of the PCI bus segments of Tal, for the purpose of providing Tal with design flexibility/scalability, functionality, and speed/performance. See Lucent Technologies, page 1, 1st and 5th paragraphs.

With regard to claim 2, it is clear that segment 802 is a PCI architecture bus.

With regard to claim 3, it is clear that segment 804 is a PCI architecture bus.

With regard to claim 6, the first bus segment operates at a substantially same bus frequency as a bus frequency of said second bus segment (see column 4, line 61 to column 5, line 5; column 6, lines 18-27).

With regard to claims 7, 16, and 25, the ORT4622 half bridge includes field programmable gate arrays (FPGAs), see page 1, 1st paragraph, and 4th paragraph.

With regard to claim 8, the first half bridge circuit and said second half bridge circuit recover a clock signal from, respectively said first bus segment and said second

bus segment (see at least column 6, lines 52-64). In any event, since the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ (see page 6, lines 20-26), it is clear that the first half bridge circuit and said second half bridge circuit recover a clock signal from, respectively said first bus segment and said second bus segment.

With regard to claims 10-12, 15-17, see discussion above regarding claims 1-3, 6, and 8.

With regard to claims 19-21, 24-26, see discussion above regarding claims 1-3, 6, and 8.

Claims 5, 14, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tal, as applied to claims 1-3, 6- 8, 10-12, 15-17, 19-21, 24- 26 above, and further in view of the following.

Tal, as discussed above, discloses the claimed invention. Tal does not disclose that the bus operating frequencies of PCI bus segment (802) and PCI bus segment (804) may be different. However, the use of two PCI buses having different frequencies is old and well-known as evidenced by at least Lange et al. Lange clearly discloses that the bridge (PCI bridge connected to PCI buses according to PCI specification) can have a bus width of either 32 bits or 64 bits. See at least column 3, lines 54-60. According to the PCI specification, PCI is operated at 33 MHz using a 32-bit-wide path; and the speed can be increased from 33 MHz to 66 MHz and the bit count can be doubled to 64. Currently, PCI-X provides for 64-bit transfers at a speed of 133 MHz.

Bus Type	Bus Width	Bus Speed	MB/sec
ISA	16 bits	8 MHz	16 MBps
EISA	32 bits	8 MHz	32 MBps
VL-bus	32 bits	25 MHz	100 MBps
VL-bus	32 bits	33 MHz	132 MBps
PCI	32 bits	33 MHz	132 MBps
PCI	64 bits	33 MHz	264 MBps
PCI	64 bits	66 MHz	512 MBps
PCI	64 bits	133 MHz	1 GBps

From the table above, it is clear that the buses can be operated under different speed, either 33 Mhz or 66 Mhz.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use two PCI buses having different frequencies, since the Examiner takes Official Notice that the use of two PCI buses having different frequencies is old and well-known as evidenced by at least Lange et al, and providing Tai with two PCI buses having different frequencies only involves ordinary skill in the art.

Claims 1-3, 5, 7, 8, 10-12, 14, 16, 17, 19-21, 23, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lange et al. in view of Lucent Technologies.

With regard to claims 1-3, Lange discloses a system for interconnecting two or more computer bus architectures, comprising: a first bus segment (primary PCI bus 12,

Figs. 2 and 4) to transmit data information; a first half bridge circuit (126, Figs. 2 and 4, column 5, lines 45-55) connected to the first bus segment (primary PCI bus 12, Figs. 2 and 4); a second bus segment (secondary PCI bus 14, Figs. 2 and 4) to transmit data information; a second half bridge circuit (127, Fig. 2, column 5, lines 45-55) connected to the first half bridge circuit (126, Figs. 2 and 4, column 5, lines 45-55) and the second bus segment (secondary PCI bus 14, Figs. 2 and 4) for transferring data information between the first half bridge circuit (126, Figs. 2 and 4, column 5, lines 45-55) and the second bus segment (secondary PCI bus 14, Figs. 2 and 4). In addition, Lange et al. also discloses that the first half bridge segment (12) and the second half bridge segment (14) communicate with a high speed serial line protocol (see at least col. 5, lines 49-51). Note that the serial line protocol includes a plurality of signal lines or data paths, see at least Fig. 2.

However, Lange does not disclose that the signal lines (provided by serial line protocol, see at least col. 5, lines 49-51, and Fig. 2) are "scalable" depending on a bandwidth needed for a particular application. To define the term "scalable", Applicants cited page 10, lines 6-10 of originally filed specification, which states that "[a]lthough the present invention is described with reference to embodiments teaching four high speed serial data lines running between two half bridge circuits, the principles of the present invention are equally applicable to the addition or subtraction of high speed serial data lines depending upon the bandwidth needed between two half bridge circuits." See Appeal Brief, Summary of the Invention, last three lines.

Lucent Technologies discloses the use of the ORT4622 half bridge (page 1, 4th paragraph) including field programmable gate arrays (FPGAs), see page 1, 1st paragraph, and containing "a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used), see page1, 4th paragraph, for providing design flexibility, functionality, and performance. See page 1, 1st and 5th paragraphs. The ORT4622 half bridge is clearly "scalable" depending on the bandwidth needed. The fact that the ORT4622 half bridge contains "a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used)" (emphasis added) clearly indicates that less than 4 channels can be used when less bandwidth is needed. As a matter of fact, the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ. Applicants clearly disclose that "[t]he first and second half bridge circuits, 4 and 6, would consist of an ORT4622 Lucent FPSC (Field Programmable System Chip) which implements a 2.5 Gb/s physical (LVDS Serial I/Os with clock recovery) and transport layers together with a PCI controller. Although the ORT4622 is shown, any number of components supporting high speed data transfer between bus segments could be used to implement the invention." See Figs 1 and 2, and Applicants' originally filed specification, page 6, lines 20-26. Since the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ, it is clear that the serial data paths provided by the two ORT4622 half bridges are "scalable" depending on a bandwidth needed.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the ORT4622 half bridge, as taught by Lucent

Technologies, to replace the half bridge 126 and 127 on each side of the PCI bus segments of Lange, for the purpose of providing Lange with design flexibility/scalability, functionality, and speed/performance. See Lucent Technologies, page 1, 1st and 5th paragraphs.

With regard to claims 5, 14, 23, Lange clearly discloses that the bridge (PCI bridge connected to PCI buses according to PCI specification) can have a bus width of either 32 bits or 64 bits. See at least column 3, lines 54-60. According to the PCI specification, PCI is operated at 33 MHz using a 32-bit-wide path; and the speed can be increased from 33 MHz to 66 MHz and the bit count can be doubled to 64. Currently, PCI-X provides for 64-bit transfers at a speed of 133 MHz.

Bus Type	Bus Width	Bus Speed	MB/sec
ISA	16 bits	8 MHz	16 MBps
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VL-bus	32 bits	33 MHz	132 MBps
PCI	32 bits	33 MHz	132 MBps
PCI	64 bits	33 MHz	264 MBps
PCI	64 bits	66 MHz	512 MBps
PCI	64 bits	133 MHz	1 GBps

From the table above, it is clear that the buses can be operated under different speed, either 33 Mhz or 66 Mhz.

With regard to claims 7, 16, and 25, the ORT4622 half bridge includes field programmable gate arrays (FPGAs), see page 1, 1st paragraph, and 4th paragraph.

With regard to claims 8, 17, and 26, since the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ (see page 6, lines 20-26), it is clear that the first half bridge circuit and said second half bridge circuit recover a clock signal from, respectively said first bus segment and said second bus segment.

With regard to claims 10-12, 14, 18, see discussion above.

With regard to claims 19-21, and 23, see discussion above.

Claims 6, 15, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lange et al., 1-3, 5, 7, 8, 10-12, 14, 16, 17, 19-21, 23, 25, and 26, and further in view of the following.

Lange et al., as discussed above, discloses the claimed invention. Lange et al. does not disclose that the bus operating frequencies of PCI bus (2) and PCI bus (4) may be substantially the same. However, the use of two PCI buses having substantially same frequencies is old and well-known as evidenced by at least Tal. Tal discloses that the first PCI bus segment operates at a substantially same bus frequency as a bus frequency of said second PCI bus segment (see column 4, line 61 to column 5, line 5; column 6, lines 18-27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use two PCI buses having substantially same frequencies, since the Examiner takes Official Notice that the use of two PCI buses having substantially

same frequencies is old and well-known as evidenced by at least Tal (see column 4, line 61 to column 5, line 5; column 6, lines 18-27); and therefore, providing Lange et al. with two PCI buses having substantially same frequencies only involves ordinary skill in the art.

Response to Arguments

Applicants' arguments filed 05/01/2006 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997)*. In fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.,* 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

103 Rejection: Tal in view of Lucent ORT4622 half bridge

On page 9, 1st paragraph of the "Remarks," Applicants argue that "Lucent Technologies appears to disclose the OR14622 that has four channels each being 622 megabit-per-second, 2.5 gbps when all 4 channels are used (See page 1). Thus, although Lucent Technologies discloses the scalability of the OR74622 chip, Lucent Technologies fails to disclose or suggest connection of two ORT4622s, much less disclose or suggest a method and apparatus relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are scalable depending on a bandwidth needed for a particular application, as recited by claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26."

In response to Applicants' argument, at the outset, it is important to note that Applicants conceded that Lucent Technologies discloses the scalability of the OR74622 half bridge.

Further, contrary to Applicants' argument, the Lucent OR74622 PCI-PCI half bridge, as its name implies, has to be employed **in pair.** Instead of using a PCI bridge connecting the two PCI buses, one can use a half PCI bridge, each connected to a respective PCI bus. Thus, 1 PCI bridge = 2 X half PCI bridges. As a matter of fact, it is well-defined in the field of computer architecture that a half bridge is used in pair. For example, US Patent No. 6,687,779 discloses the use of a PCI half bridge that can be used a primary or secondary part of a PCI bridge. Each half bridge is connected to a respective PCI bus (see at least column 3, line 66 to column 4, line 5). Another example

is the disclosure of US Patent No. 6,968,464 describing the use of a pair of PCI half bridge as disclosed in US Patent No. 6,070,214. Specifically, US Patent No. 6,968,464 discloses that "U.S. Pat. No. 6,070,214 assigned to Mobility Electronics also describes a "split bridge" implementation. A split bridge may allow the extension of a computer bus, such as a PCI bus, to a remote location with little or no performance degradation or software requirements. For example, standard PCI--PCI bridge chip functionality may be split between two remotely located components which may be located on the computer and the remote chassis, respectively. For example, in a PCI split bridge system, the host computer includes a primary PCI bus and a first interface comprising a first portion of the bridge, the remote system includes a secondary PCI bus and a second interface comprising a second portion of the bridge, and the two systems are coupled via a transmission medium, e.g., a serial or parallel transmission cable. The first interface, the transmission medium, and the second interface may collectively comprise the bridge. In this manner, PCI devices attached to both of the PCI systems may be coupled seamlessly, or transparently, i.e., the PCI expansion devices coupled to the remote PCI bus may appear to the computer system as if they were coupled directly to the local PCI bus in the host computer system. One added benefit of this approach is the expansion of the number of PCI devices which may be included in the overall system, normally limited to 3 or 4 PCI devices. Of course, this technique is not limited to PCI based systems, and may be used with other buses as well, such as Compact PCI, PXI, VME or VXI, among others" (see column 2, lines 20-47).

Thus, it is clear that the Lucent ORT4622 PCI half bridge is used in pair, each ORT4622 PCI half bridge is connected to a first PCI bus segment and a second PCI bus segment of Tal.

Applicants also argue that "the Examiner alleges that 'the Lucent Technologies' OR14622 half bridge is the same OR14622 half bridge that the Applicants employ.' (Examiner's Answer, page 7). The reason Lucent Technologies' OR14622 is the same OR14622 that Applicants employ is that the Examiner simply found a reference that reiterates what Applicants disclose in their specification. The Applicants are unsure of what purpose finding a prior art reference to reiterate what Applicants disclose in their specification served. Lucent Technologies STILL fails to disclose or suggest connection of TWO half bridge circuits for any reason, much less disclose or suggest a method and apparatus relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are scalable depending on a bandwidth needed for a particular application, as recited by claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26."

In response to Applicants' argument, at the outset, it is important to note that Applicants conceded that the Lucent Technologies' OR14622 half bridge is the same OR14622 half bridge that the Applicants employ.

Further, contrary to Applicants' argument, Lucent does disclose the use of a PCI half bridge (see discussion above). Also, as noted above, the PCI half bridge, as well-defined in the field of computer architecture, must be used in **pair**. Still further, the

rejection is based on a combination of references. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). As already conceded by Applicants that the Lucent PCI half bridge is scalable depending on a particular bandwidth, Lucent Technologies discloses the use of the ORT4622 half bridge (page 1, 4th paragraph) including field programmable gate arrays (FPGAs), see page 1, 1st paragraph, and containing "a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used), see page1, 4th paragraph, for providing design flexibility, functionality, and performance. See page 1, 1st and 5th paragraphs. The ORT4622 half bridge is clearly "scalable" depending on the bandwidth needed. The fact that the ORT4622 half bridge contains "a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used)" (emphasis added) clearly indicates that less than 4 channels can be used when less bandwidth is needed. As a matter of fact, the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ. Applicants clearly disclose that "[t]he first and second half bridge circuits, 4 and 6, would consist of an ORT4622 Lucent FPSC (Field Programmable System Chip) which implements a 2.5 Gb/s physical (LVDS Serial I/Os with clock recovery) and transport layers together with a PCI controller. Although the ORT4622 is shown, any number of components supporting high speed data transfer between bus segments could be used to implement the invention." See Figs 1 and 2, and Applicants' originally filed specification, page 6, lines 20-26. Since the Lucent Technologies' ORT4622 half bridge

is the same ORT4622 half bridge that Applicants employ, it is clear that the serial data paths provided by the two ORT4622 half bridges are "scalable" depending on a bandwidth needed.

Thus, it is clear that the combination of Tal and Lucent ORT4622 PCI half bridge would provide a method and apparatus relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are scalable depending on a bandwidth needed for a particular application.

In addition, Applicants argue that "Nothing within Tal nor Lucent Technologies suggests modifying Tal to replace Tal's disclosed PCI serialized with two ORT4622s. Thus, any modification of Tal without some suggested need to simply arrive at the claimed features is based on improper hindsight. Moreover, the Examiner alleged that the motivation to modify Tal to replace the half bridge on each side of the PCI bus segments of Tal is to provide flexibility/scalability, functionality, and speed/performance as disclosed by Lucent Technologies (See Examiner's Answer, page 7). However, the Examiner's motivation to modify Tal is simply Lucent Technologies disclosed benefits associated with the ORT4622 chip. The Examiner has still failed to provide motivation why one of ordinary skill in the art would be motivated to modify Tal that fails to disclose any deficiencies that would suggest such a modification."

Contrary to Applicants' argument, the motivation for the combination of Tal and Lucent ORT4622 half bridge is clearly set forth in the 35 USC 103 rejection. As clearly stated in the rejection, "It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the ORT4622 half bridge, as taught by

Lucent Technologies, to replace the half bridge 700 (Figs. 7 and 8) on each side of the PCI bus segments of Tal, for the purpose of providing Tal with design flexibility/scalability, functionality, and speed/performance. See Lucent Technologies, page 1, 1st and 5th paragraphs" (emphasis added). Applicants are also reminded that obviousness can be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988), and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, as stated above, it is clear that the motivation for the combination of Tal and Lucent ORT4622 half bridge is clearly set forth in the 35 USC 103 rejection. Further, as set forth in MPEP Section 2144, "the strongest rationale for combining references is a recognition, expressly or impliedly in the prior art or drawn from a convincing line of reasoning based on established scientific principles or legal precedent, that some advantage or expected beneficial result would have been produced by their combination. *In re Sernaker*, 702 F.2d 989, 994-95, 217 USPQ 1, 5-6 (Fed. Cir. 1983)." In the instant case, the advantage or expected beneficial result, which would have been produced by the combination, is design flexibility/scalability, functionality, and speed/performance.

Applicants also argue that "the Examiner had failed to provide support for the allegation that CompactPCI and FPGAs are scaleable."

In response to Applicants' argument, as noted above, the rejection is based on a combination of references. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). As already conceded by Applicants that the Lucent PCI half bridge is scalable depending on a particular bandwidth, it is clear that the combination of Tal and Lucent ORT4622 PCI half bridge would provide a method and apparatus relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are scalable depending on a bandwidth needed for a particular application.

With regard to claims 5, 14, and 23, Applicants argue that

"Lange is relied on to disclose PCI buses operating at difference frequencies (See Examiner's Answer, page 9). However, as discussed below the Examiner acknowledges that Lange fails to disclose "scaleable" signal lines (See Examiner's Answer, page 11). Thus, Tal which the Examiner acknowledges fails to disclose "scaleable" signal lines in view of Lange which the Examiner acknowledges fails to disclose "scaleable" signal lines would STILL fail to disclose or suggest "scaleable" signal lines, i.e., a method and apparatus relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are scalable depending on a bandwidth needed for a particular application, as recited by claims 5, 14 and 23."

In response to Applicants' argument, Applicants again are reminded that the rejection is based on a combination of references. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). As already conceded by Applicants that the Lucent PCI half bridge is scalable depending on a particular bandwidth, it is clear that the combination of Tal and Lucent ORT4622 PCI half bridge would provide a method and apparatus relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are scalable depending on a bandwidth needed for a particular application. As acknowledged by Applicants, Lange is relied on to disclose PCI buses operating at difference frequencies.

The 103 Rejection (Lange in view of Lucent Technologies)

At the outset, it is noted that Applicants lumped all rejected claims 1-3, 5-8, 10-12, 14-17. 19-21, and 23--26 under the header, "claims 1-3, 5-8, 10-12, 14-17. 19-21, and 23-26 over Lanqe in view of Lucent Technologies and Official Notice." This is incorrect, since these claims are rejected under different rejections. In fact, claims 1-3, 5, 7, 8, 10-12, 14, 16, 17, 19-21, 23, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tal in view of Lucent Technologies. The Official Notice (with supportive evidence) is only applied to claims 6, 15, and 24.

With regard to claims 1-3, 5, 7, 8, 10-12, 14, 16, 17, 19-21, 23, 25, and 26, Applicants argue that "Lucent Technologies fails to disclose or suggest the application scalability to connection of two half bridge circuits, i.e., fails to disclose or suggest a method and apparatus relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are scalable depending on a bandwidth needed for a particular application, as recited by claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26."

In response to Applicants' argument, at the outset, it is important to note that Applicants already conceded that Lucent Technologies discloses the scalability of the OR74622 half bridge (see above).

Further, contrary to Applicants' argument, the Lucent OR74622 PCI-PCI half bridge, as its name implies, has to be employed **in pair.** Instead of using a PCI bridge connecting the two PCI buses, one can use a half PCI bridge, each connected to a respective PCI bus. Thus, 1 PCI bridge = 2 X half PCI bridges. As a matter of fact, it is well-defined in the field of computer architecture that a half bridge is used in pair. For example, US Patent No. 6,687,779 discloses the use of a PCI half bridge that can be used a primary or secondary part of a PCI bridge. Each half bridge is connected to a respective PCI bus (see at least column 3, line 66 to column 4, line 5). Another example is the disclosure of US Patent No. 6,968,464 describing the use of a pair of PCI half bridge as disclosed in US Patent No. 6,070,214. Specifically, US Patent No. 6,968,464 discloses that "U.S. Pat. No. 6,070,214 assigned to Mobility Electronics also describes

a "split bridge" implementation. A split bridge may allow the extension of a computer bus, such as a PCI bus, to a remote location with little or no performance degradation or software requirements. For example, standard PCI--PCI bridge chip functionality may be split between two remotely located components which may be located on the computer and the remote chassis, respectively. For example, in a PCI split bridge system, the host computer includes a primary PCI bus and a first interface comprising a first portion of the bridge, the remote system includes a secondary PCI bus and a second interface comprising a second portion of the bridge, and the two systems are coupled via a transmission medium, e.g., a serial or parallel transmission cable. The first interface, the transmission medium, and the second interface may collectively comprise the bridge. In this manner, PCI devices attached to both of the PCI systems may be coupled seamlessly, or transparently, i.e., the PCI expansion devices coupled to the remote PCI bus may appear to the computer system as if they were coupled directly to the local PCI bus in the host computer system. One added benefit of this approach is the expansion of the number of PCI devices which may be included in the overall system, normally limited to 3 or 4 PCI devices. Of course, this technique is not limited to PCI based systems, and may be used with other buses as well, such as Compact PCI, PXI, VME or VXI, among others" (see column 2, lines 20-47).

Thus, it is clear that the Lucent ORT4622 PCI half bridge is used in pair, each ORT4622 PCI half bridge is connected to a first PCI bus segment and a second PCI bus segment of Lange.

Applicants also argue that "the Examiner alleges that "the

Lucent Technologies' OR14622 half bridge is the same OR14622 half bridge that the Applicants employ." (Examiner's Answer, page 7). The reason Lucent Technologies' 0RT4622 is the same ORT4622 that Applicants employ is that the Examiner simply found a reference that reiterates what Applicants disclose in their specification. The Applicants are unsure of what purpose finding a prior art reference to reiterate what Applicants disclose in their specification served. Lucent Technologies STILL fails to disclose or suggest connection of two half bridge circuits for any reason, much less disclose or suggest a method and apparatus relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are scalable depending on a bandwidth needed for a particular application, as recited by claims 1-3, 5-8, 10-12, 14-17, 19-21,and 23-26."

In response to Applicants' argument, at the outset, it is important to note that Applicants conceded that the Lucent Technologies' OR14622 half bridge is the same OR14622 half bridge that the Applicants employ.

Further, contrary to Applicants' argument, Lucent does disclose the use of a PCI half bridge (see discussion above). Also, as noted above, the PCI half bridge, as well-defined in the field of computer architecture, must be used in **pair**. Still further, the rejection is based on a combination of references. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). As already conceded by

Applicants that the Lucent PCI half bridge is scalable depending on a particular bandwidth, Lucent Technologies discloses the use of the ORT4622 half bridge (page 1, 4th paragraph) including field programmable gate arrays (FPGAs), see page 1, 1st paragraph, and containing "a 4-channel 622 megabit-per-second **(2.5 gbps when all 4 channels are used)**, see page1, 4th paragraph, for providing design flexibility, functionality, and performance. See page 1, 1st and 5th paragraphs. The ORT4622 half bridge is clearly "scalable" depending on the bandwidth needed. The fact that the ORT4622 half bridge contains "a 4-channel 622 megabit-per-second (**2.5 gbps when all 4 channels are used)**" (emphasis added) clearly indicates that less than 4 channels can be used when less bandwidth is needed. As a matter of fact, **the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ**. Applicants clearly disclose that "[t]he first and second half bridge circuits, 4 and 6, would consist of an ORT4622 Lucent FPSC (Field Programmable System Chip) which implements a 2.5 Gb/s physical (LVDS Serial I/Os with clock recovery) and transport layers together with a PCI controller. Although the ORT4622 is shown, any number of components supporting high speed data transfer between bus segments could be used to implement the invention." See Figs 1 and 2, and Applicants' originally filed specification, page 6, lines 20-26. Since **the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ**, it is clear that the serial data paths provided by the two ORT4622 half bridges are "scalable" depending on a bandwidth needed.

In addition, Applicants argue that "Nothing within Lange nor Lucent Technologies suggests modifying Lange to replace Lange's disclosed primary bridge and secondary bridge with two ORT4622s. Thus, any modification of Lange without some suggested need to simply arrive at the claimed features is based on improper hindsight."

Contrary to Applicants' argument, the motivation for the combination of Lange and Lucent ORT4622 half bridge is clearly set forth in the 35 USC 103 rejection. As clearly stated in the rejection, "It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the ORT4622 half bridge, as taught by Lucent Technologies, to replace the half bridge 126 and 127 on each side of the PCI bus segments of Lange, for the purpose of providing Lange with design flexibility/scalability, functionality, and speed/performance. See Lucent Technologies, page 1, 1st and 5th paragraphs" (emphasis added). Applicants are also reminded that obviousness can be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988), and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, as stated above, it is clear that the motivation for the combination of Lange and Lucent ORT4622 half bridge is clearly set forth in the 35 USC 103 rejection. Further, as set forth in MPEP Section 2144, "the strongest rationale for combining references is a recognition, expressly or impliedly in the prior art or drawn from a convincing line of reasoning based on established scientific principles or legal

precedent, that some advantage or expected beneficial result would have been produced by their combination. *In re Semaker*, 702 F.2d 989, 994-95, 217 USPQ 1, 5-6 (Fed. Cir. 1983)." In the instant case, the advantage or expected beneficial result, which would have been produced by the combination of Lange and Lucent, is design flexibility/scalability, and speed/performance.

Applicants also argue that Official Notice is relied on to disclose two PCI buses having substantially same frequencies. Thus, Lange even in view of two PCI buses having substantially same frequencies STILL fails to disclose or suggest scalable signal lines between TWO half bridge circuits, i.e., fails to disclose or suggest a method and apparatus relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are scalable depending on a bandwidth needed for a particular application, as recited by claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26."

In response to Applicants' argument, at the outset, it is noted that **the Official Notice (with supportive evidence) is only applied to claims 6, 15, and 24.**

With regard to claims 6, 15, and 24, Applicants again are reminded that the rejection is based on a combination of references. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). As already conceded by Applicants that the Lucent PCI half bridge is scalable depending on a particular bandwidth, it is clear that the combination of Lange and Lucent ORT4622 PCI half bridge would provide a method and apparatus relying on a plurality of data paths used

to connect a first half bridge circuit and a second half bridge circuit that are scalable depending on a bandwidth needed for a particular application. As acknowledged by Applicants, the Official Notice (with supportive evidence) is relied on to disclose PCI buses operating at same frequencies.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Dang whose telephone number is 571-272-3626. The examiner can normally be reached on Monday-Friday from 9:AM to 5:PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart, can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Khanh Dang
Primary Examiner